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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,193	02/13/2002	Shenlin Chen	MI22-1927	8017

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EXAMINER	
HUYNH, YENNHU B	
ART UNIT	**PAPER NUMBER**
2813	

DATE MAILED: 07/26/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/075,193	CHEN ET AL.	
	Examiner	Art Unit	
	Yennhu B. Huynh	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 February 2004*.

2a)☒ This action is **FINAL**. 2b)☒ This action is non-final. CDR July 2004

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *42-48* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *42-48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Applicant paper filed on 2/17/04.

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 8/27/03 has been entered.

Currently, claims 42-48 are pending.

Information Disclosure Statement

The information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 42-48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Al-Brown (U.S. 5418,180) in view of Figura et al. (U.S. 5,661,064) and DeBoer et al. (U.S. 6,046,093).

Brown at figs. 1-8 in related text col. 1-8 discloses a process for fabricating storage capacitor structure, which include:

-Re. claim 42: forming a container structure (fig.21) comprising a multiple silicon containing layer of first silicon containing layer 31, center silicon containing layer 32 & last silicon containing layer 41 (fig. 4, col.6 lines 6-8); the last silicon containing layer defining and inner periphery of the container and the first silicon containing layer defining an outer periphery of the container; wherein the first silicon containing layer 31 being doped with conductive enhancing n type dopant such as arsenic, phosphorous or boron (col. 4, lines 3-8); converting at least some of each of the first and last silicon containing layers to HSG silicon (fig. 7a, col. 4 & 5 lines 61-15); forming a dielectric material layer 81 along the exposed inner and exposed outer peripheries of the container construction; forming a conductive material layer 82 over the dielectric material, the container structure and conductive material together defining capacitor structure (fig.8, col.6, lines 6-28).

However, Brown does not disclose wherein the first silicon containing layer being more heavily doped than the second (last) silicon-containing layer.

Figura et al. at figs. 1-10 in related text col. 1-12 disclose a method of forming a capacitor having container member, which include wherein the first silicon containing layer 20 or 28 being less heavily doped than the second silicon containing layer 24 or 32 of the container 34 or 35 (col. 3 lines 26-68). However, Figura et al. also disclose the heavily doped and lightly doped layers between the first and second silicon containing layer 20,24,28 & 32 can be reversed (col.5 lines 1-16).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Brown invention by incorporation the first silicon containing layer being heavily doped than the second (last) silicon containing layer, because the first silicon layer is defined as an outer periphery of the capacitor container, which function as a part of capacitor electrode, therefore, the that heavily doped first silicon layer will provide high electrically conductive for electrical connection to transistor gate or incorporation into DRAM cell.

Brown also do not disclose wherein the HSG silicon from the first silicon containing layer /outer periphery of the container having smaller average grain size than the HSG silicon from the last (or second) silicon containing layer/inner periphery of the container.

Deboer et al. at figs. 11-15 in related text col. 1-14 disclose a method of forming capacitors, which include the HSG silicon layer having larger average grain size if the HSG formed over the inner surface of capacitor container structure (col.6, lines 53-68).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine Brown invention by incorporation HSG silicon from the first silicon containing layer/outer periphery of the container having smaller average grain size than the last silicon containing layer/inner periphery of the container, to void a risk of shorting between the container and other structures when the outer surface is small size grain or smooth, and to increase the surface area of electrodes, when the

inner surface is large grain size, in related association to those which would occur without rugged inner surface were utilized.

Brown also disclose:

-Re. claim 48: wherein the last (or second) silicon-containing layer is substantially undoped (col.7, cls. 21 & 24).

Brown, Figura et al. and DeBoer et al. disclose substantially all of the claimed invention. However, they do not disclose wherein exposing the first and second (last) silicon containing layer in a range of temperature at least about 550° for a time less or equal to about 2 minutes, and less than or equal to about $1x10^{-4}$ Torr to seed the silicon containing layers (cl.43), and an average dopant concentration to the first and second (last) silicon layer (cls. 44-47).

-Re. claim 43: DeBower et al. discloses only wherein the silicon-containing layers are annealed at a temperature, which is from 450°C to 560°C (col.5, lines 55-65).

With respect to claims 43-47 the range of time, pressure and concentration dopant are considered to involve routine optimization while has been held to be within the level of ordinary skill in the art, as noted In re Aller 105 USPQ233, 255 (CCPA 1955). the selection of reaction parameters such as temperature and concentration would have been obvious.

"Normally, it is to expected that a change in temperature, or in range, concentration, cycles, thickness, would be an unpatentable modification. Under some circumstance, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art ... such ranges are termed "critical ranges and the applicant has the burden of proving such criticality ... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller 105 USPQ233, 255 (CCPA 1955). See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

Response to Arguments

Applicant's arguments filed on 2/17/04 been fully considered but they are not persuasive.

Applicant argues that Brown disclose specifically a layer of TiN material to coat HSG, which together form a storage node cell plate.

The Brown 's TiN layer just coat to the HSG, after the first silicon layer 31 convert to the HSG, therefore the TiN just to enhance the capacitor storage node. The TiN does not formed together with the first silicon layer 31, and then the both TiN and the first silicon layer 31 is converted to HSG.

However, in claim 42 recite the container construction comprising first and second silicon containing layer, wherein the first and second silicon layer converting to the HSG. Brown disclose the container construction comprising three silicon containing layers, and wherein the first and last silicon layer converting to the HSG and any inner

silicon layer do not penetrate the silicon interface layers. Therefore, Brown discloses completely limitations recites in claim 42.

Applicant also argues that Brown, Deboer and Figura do not disclose forming "a dielectric material along an exposed inner and an exposed outer periphery of a container construction where the exposed inner periphery of the container is defined by a second silicon containing layer and the exposed outer periphery of the container is defined by a first silicon containing layer", which claim 42 recited.

In claim 42 recited " forming a dielectric material along the inner and outer peripheries of the container construction" only, and do not recite the limitation: "where the exposed inner periphery of the container is defined by a second silicon containing layer and the exposed outer periphery of the container is defined by a first silicon containing layer".

Brown discloses clearly forming a dielectric material layer 81 along the exposed inner and exposed outer peripheries of the container construction (fig.8).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yennhu Huynh whose telephone number is 571-272-1692. The examiner can normally be reached on Monday-Friday from 8:00 AM to 4.30PM.

If attempts to reach the examiner by telephone are unsuccessfully, the Examiner's supervisor, Carl Whitehead, Jr., can be reached on 571-272-1702 The fax phone number for the organization where this application or proceeding is assigned is (703) 308-3432.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

YNBH,

071104

CARL WHITEHEAD, JR.
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800